WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a plurality of chips, which are integrally sealed;

a test signal input terminal for receiving an externally supplied test signal;

a test result output terminal for outputting a test result of said plurality of chips to outside; and

control signal input terminals for receiving externally supplied test control signals,

the test signal inputted from said test signal input terminal being successively transferred through said plurality of chips, and

the test control signals inputted from said control signal input terminals being individually supplied to each of said plurality of chips.

2. The semiconductor device as set forth in claim 1, wherein said plurality of chips are connected to each other via said test result output terminal.

3. A semiconductor device, comprising:

a plurality of chips, which are integrally sealed;

a test signal input terminal for receiving an externally supplied test signal;

a test result output terminal for outputting a test

result of said plurality of chips to outside; and

control signal input terminals for receiving externally supplied test control signals,

only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals,

the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result to outside, and

the test control signals being individually supplied from the one of said plurality of chips to each of the other chips.

4. The semiconductor device as set forth in claim 3, wherein only the one of said plurality of chips includes a controller for controlling an input/output interface of the test signal.

5. A semiconductor device in which a plurality of chips are integrally sealed, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

Sub C1

a control circuit for controlling said test register for testing the chip, test commands/data input and output terminals connected to said control circuit, and input terminals of signals to be used in the test, which are all mounted on each chip,

a test commands/data input terminal of a device being connected to the test commands/data input terminal of a chip of a first stage, and the test commands/data output terminal of a chip of a preceding stage being serially connected to the test commands/data input terminal of a chip of a following stage, and the test commands/data output terminal of a chip of a last stage being connected to a test commands/data output terminal of the device, and input terminals of the device for the signals to be used in the test being connected to the corresponding input terminals of the signals of each chip.

6. A semiconductor device in which a plurality of chips are integrally sealed, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output terminals connected to said control circuit, and input

terminals of signals, connected to said control circuit, to be used in the test, which are all mounted on each chip,

a test commands/data input terminal of a device being connected to the test commands/data input terminal of a chip of a first stage, and the test commands/data output terminal of each chip being connected to a corresponding output terminal of the device and serially to the test commands/data input terminal of a chip of a following stage via the output terminal of the device, and input terminals of the device for the signals to be used in the test being connected to the corresponding input terminals of the signals of each chip.

7. A semiconductor device in which a plurality of chips are integrally sealed, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling the test register for testing the chip, test commands/data relay input and output terminals connected to said control circuit, and output terminals of signals to be used in the test outputted from the control circuit, which are all mounted on a chip of a first stage,

test commands/data input and output terminals of a

device being respectively connected to the test commands/data input and output terminals of the chip of the first stage, and the relay output terminal of the chip of the first stage being connected to a test commands/data input terminal of a chip of a following stage, and a test commands/data output terminal and a test commands/data input terminal being serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output terminal of a chip of a last stage being connected to the relay input terminal of the chip of the first stage so as to form a loop, and the output terminals of the chip of the first stage for the signals to be used in the test being connected to input terminals of the signals of the other chips.